Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Confirmation No. 6948

Application No.:	10/671,203
Filing Date:	September 24, 2003
Appellant:	Jeffrey L. Wise et al.
Group Art Unit:	2616
Examiner:	Redentor M. Pasia
Title:	METHOD OF UPDATING FLOW CONTROL WHILE REVERSE LINK IS IDLE
Attorney Docket:	1400B-000019/US

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AMENDED BRIEF ON APPEAL

Sir:

This is an appeal to the Board of Patent Appeals and Interferences from a final decision of Examiner Pasia mailed January 8, 2008 and Advisory Action mailed July 21, 2008 wherein claims 1-5, 7-12, 14-20 and 22-23 were finally rejected. A Notice of Appeal was timely filed in the Patent and Trademark Office on July 7, 2008.

I. Real Party in Interest

The real party in interest in this matter is Emerson Network Power - Embedded Computing, Inc., having a place of business at 8310 Excelsior Drive Madison, Wisconsin 53717.

II. Related Appeals and Interferences

To Appellants' knowledge, there are no related appeals or interferences.

III. Status of the Claims

Claims 1-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 5-8 of co-pending Application No. 10/671,204. Claims 9-12 and 14-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17, 19, and 21-26 of co-pending Application No. 10/671,204. Claims 1-5, 7-12, 14-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US 6,922,408 B2) in view of Jones et al. (US 6,944,173 B1) in further view of Takase et al. (US 7,023,799 B2). Claims 6, 13 and 21 have been cancelled.

Therefore, Claims 1-5, 7-12, 14-20 and 22-23 are currrently pending, were finally rejected in the application and are appealed herein.

IV. Status of Amendments

Pursuant to the Advisory Action dated July 21, 2008, Appellant's Amendment submitted on July 7, 2008 has been entered by the Examiner.

V. Summary of Claimed Subject Matter

The present application is directed to a system and method for controlling information flow in a computer network, e.g., a switch fabric network.

A switch fabric network may have any number of end nodes connected to each other through a switch fabric, which may comprise one or more switches and/or routers. See, e.g., Application, pg. 3, lines 16-19. Each connection between the switches and the end nodes is a point-to-point serial connection. Data exchanged in the switch fabric network can be in the form of packets. See, e.g., Application, pg. 3, lines 16-21.

The switches may be represented as a link transmitter and a link receiver, which are connected by ingress links that can be bi-directional, i.e., having a forward and reverse link. See, Application, pg. 4, lines 27 to pg. 5, line 2. A packet is transmitted from a link transmitter to a link receiver over the forward link, while a flow control packet is transmitted from the link receiver to the link transmitter over the reverse link. See, e.g., Id.

The flow of information over a network may be controlled using a credit based link control scheme. See, e.g., Application, pg. 5, lines 3-12. The packets exchanged may be transmitted over a plurality of logical channels. See, e.g., Application, pg. 5, lines 24-31. In a credit-based link flow control scheme, the link receiver provides a plurality of data credits to a link transmitter. See, e.g., Application, pg. 6, lines 8-9. These data credits represent empty space that is ready to receive a packet. See, e.g., Application, pg. 6, lines 8-15. As a packet is transmitted from the link transmitter to a link receiver, a link transmitter flow control algorithm ensures that the amount of data credits is updated such that packets will not be lost. The link transmitter flow control algorithm will allow the link transmitter to continue to transmit information packets to the link receiver so long as there are data credits available. See, e.g., Application, pg. 6, lines 16-27. If the amount of data credits is diminished or reaches a low threshold level, the link transmitter will cease transmitting information packets to the link receiver. See, e.g., Id. This prevents the link receiver from becoming oversubscribed. See, e.g., Id.

Of particular relevance to this application, the link transmitter selects from which of the plurality of logical channels to draw the packet. See, e.g., Application, pg. 6, lines 28-30. In this manner, the link transmitter decides how to allocate the data credits among the plurality of logical channels and also from which the plurality of logical channels to draw the packet for transmission to the link receiver. See, e.g., Application, pg. 6, lines 30-33. The link transmitter is aware of how many packets are queued up on each of the plurality of logical channels and, therefore, is in the best position to know how to allocate the data credits. See, e.g., Application, pg. 6 line to pg. 7, line 3. Thus, the link transmitter may allocate data credits more efficiently among the plurality of logical channels. See, e.g., Application, pg. 7, lines 3-6.

In the prior art, the link receiver was responsible for allocating data credits among the plurality of logical channels. See, e.g., Id. One disadvantage of this prior art method is that the

link receiver would allocate data credits to logical channels that have no traffic queued. See, e.g., Application, pg. 7, lines 7-16. In this situation, data credits would not be used immediately and may remain unused on a specific logical channel, while another logical channel has a backup of packets to be sent. See, e.g., Id. By allowing the link transmitter to allocate the data credits to the logical channels, the allocation may be based upon the transmitter link's knowledge of the traffic to be sent and, therefore, more efficient use of the ingress link may be ensured.

Appellants respectfully submit the following tables as a further summary of the claimed subject matter. The tables below include the following information: (i) a verbatim listing of each limitation of the independent claims on appeal, (ii) an identification in the drawings of an example of each limitation as illustrated in the drawings, and (iii) an identification by page and paragraph number in the disclosure of a portion of the specification that discloses each limitation.

Claim Language	Example in Drawings	Exemplary Reference in Specification
1. A method, comprising: providing from a link a receiver a plurality of data credits to a link transmitter;	"link a [sic] receiver" - FIG. 3, element 304	pg. 6, lines 8-15
	"plurality of data credits" - FIG. 3, element 320	pg. 6, lines 8-15
	"link transmitter" - FIG. 3, element 302	pg. 6, lines 8-15
allocating at the link transmitter the plurality of data credits to a plurality of logical channels;	"plurality of logical channels" - FIG. 3, element 318	pg. 6, line 28 to pg. 7, line 6
transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link, wherein the ingress link has a forward link and a reverse link, and wherein the plurality of packets are transmitted on the forward link;	"a plurality of packets" - FIG. 3, element 325	pg 4, line 27 to pg. 5, line 2
	"ingress link" - FIG. 3, element 310	pg. 4, lines 27-32
	"forward link" -	pg. 4, lines 27-32

Claim Language	Example in Drawings	Exemplary Reference in Specification
	FIG. 3, element 312	
	"reverse link" - FIG. 3, element 314	pg. 4, lines 27-32
storing the plurality of packets in a plurality of receiver buffers at the link receiver;	"a plurality of receiver buffers" - FIG. 3, element 322	pg. 5, lines 17-25
updating a free buffer pool at the link receiver; and	"free buffer pool" - FIG. 3, element 330	pg. 5, lines 17-25
transmitting a flow control packet from a link receiver to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.	"flow control packet" - FIG. 3, element 332	pg. 7, line 26 to pg, 8, line 11

Claim Language	Example in Drawings	Exemplary Reference in Specification
9. A switch, comprising:	FIG. 1, elements 102 and 104	pg. 3, lines 16-28
a plurality of receiver buffers coupled to receive a packet from a link transmitter on an ingress link having a forward link and a reverse link after the link transmitter allocates a plurality of data credits to a plurality of logical channels, wherein the packet is stored in the plurality of receiver buffers;	"receiver buffers" - FIG. 3, element 322	pg. 5, lines 17-25
	"packet" - FIG. 3, element 325	pg. 4, line 27 to pg. 5, line 2
	"link transmitter" FIG. 3, element 302	pg. 6, lines 8-15
	"ingress link" - FIG. 3, element 310	pg. 4, lines 27-32

Claim Language	Example in Drawings	Exemplary Reference in Specification
	"forward link" - FIG. 3, element 312	pg. 4, lines 27-32
	"reverse link" - FIG. 3, element 314	pg. 4, lines 27-32
a free buffer pool; and	"free buffer pool" - FIG. 3, element 330	pg. 5, lines 17-25
a link receiver flow control algorithm, wherein the link receiver flow control algorithm transmits a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.	"link receiver flow control algorithm" - FIG. 3, element 326	pg. 6, lines 16-27
	"flow control packet" - FIG. 3, element 332	pg. 7, line 26 to pg. 8, line 11

Claim Language	Example in Drawings	Exemplary Reference in Specification
16. A computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of updating a link transmitter, the instructions comprising:		pg. 4, lines 7-15
providing from a link a receiver a plurality of data credits to a link transmitter;	"link a [sic] receiver" - FIG. 3, element 304	pg. 6, lines 8-15
	"plurality of data credits" - FIG. 3, element 320	pg. 6, lines 8-15
	"link transmitter" -	pg. 6, lines 8-15

Claim Language	Example in Drawings	Exemplary Reference in Specification
	FIG. 3, element 302	
allocating at the link transmitter the plurality of data credits to a plurality of logical channels;	"plurality of logical channels" - FIG. 3, element 318	pg. 6, line 28 to pg. 7, line 6
transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link, wherein the ingress link has a forward link and a reverse link, and wherein the plurality of packets are transmitted on the forward link;	"a plurality of packets" - FIG. 3, element 325	pg 4, line 27 to pg. 5, line 2
	"ingress link" - FIG. 3, element 310	pg. 4, lines 27-32
	"forward link" - FIG. 3, element 312	pg. 4, lines 27-32
	"reverse link" - FIG. 3, element 314	pg. 4, lines 27-32
storing the plurality of packets in a plurality of receiver buffers at the link receiver;	"a plurality of receiver buffers" - FIG. 3, element 322	pg. 5, lines 17-25
updating a free buffer pool at the link receiver; and	"free buffer pool" - FIG. 3, element 330	pg. 5, lines 17-25
transmitting a flow control packet from a link receiver to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.	"flow control packet" - FIG. 3, element 332	pg. 7, line 26 to pg, 8, line 11

VI. Grounds of Rejection to be Reviewed on Appeal

The following issues are presented in this appeal:

Claims 1-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 5-8 of co-pending Application No. 10/671,204. Claims 9-12 and 14-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17, 19, and 21-26 of co-pending Application No. 10/671,204.

Claims 1-5, 7-12, 14-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US 6,922,408 B2) in view of Jones et al. (US 6,944,173 B1) in further view of Takase et al. (US 7,023,799 B2).

VII. Argument

A. Typographical Errors in Claims

Appellants note that a number of claims contain typographical errors that were mistakenly included during the prosecution of the present Application. Specifically, in the Amendment dated October 17, 2007 Appellants mistakenly amended claims 1 and 16 to include the phrase "from a link a receiver" instead of "from a link receiver" as intended. Furthermore, in the Amendment dated July 7, 2008 Appellants mistakenly included the phrase "the link receiver" in claim 2, which was previously deleted in the October 17, 2007 Amendment. Upon allowance of this Application, Appellants will file a Request for Certificate of Correction to correct these unintentional errors.

B. Double Patenting Rejections

Claims 1-8 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 5-8 of co-pending Application No. 10/671,204. Claims 9-12 and 14-23 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over

claims 17, 19, and 21-26 of co-pending Application No. 10/671,204. Appellants note that this rejection is provisional because co-pending Application No. 10/671,204 has not yet issued as a patent. Appellants elect to defer responding to this rejection until Application No. 10/671,204 has been patented.

C. The Rejection of Claims 1-5, 7-12, 14-20 and 22-23 under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. in view of Jones et al. in further view of Takase et al.

The Examiner has rejected claims 1-5, 7-12, 14-20 and 22-23 under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US 6,922,408 B2) in view of Jones et al. (US 6,944,173 B1) in further view of Takase et al. (US 7,023,799 B2).

1. The proposed combination fails to teach "allocating at the link transmitter the plurality of data credits to a plurality of logical channels"

Appellants agree with the Examiner that Bloch fails to show the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels. Appellants disagree with the Examiner's assertion, however, that the Jones reference teaches this limitation and thereby cures the acknowledged deficiency of Bloch.

The Jones reference discloses that "when the receiver 12 sends a virtual channel credit packet 22 for a particular virtual channel, the transmitter 10 knows to which virtual channel the credit packet is designated." Jones, col. 3, lns. 19-21. Jones further states that:

> The receiver 12 first checks if there is any available buffer for VCN "N" (block 34). If the receiver 12 does not have any buffer available for transmission (block 36), it waits for a predetermined time and rechecks for available buffer until it finds some buffer (block 34). Once available buffer is found (block 36), then the receiver 12 sends a virtual channel credit packet 22 for VCN "N" to the transmitter (block 38).

Jones, col. 3, lns. 44-49 (emphasis added). In other words, Jones discloses allocation of data credits to a plurality of logical channels at the link receiver. Thus, in the combination of Bloch and Jones, any allocation occurs at the receiver, and the transmitter simply responds to the allocation already determined by the receiver. The claims at issue, however, are directed to allocating at the link transmitter the plurality of data credits to a plurality of logical channels.

In the Advisory Action mailed July 21, 2008, the Examiner acknowledges that the combination of Bloch and Jones fails to disclose allocation occurring at the transmitter. See, Advisory Action, pg. 3 (if the "allocation [of data credits] occurs at the transmitter, then the rejection of Bloch in view of Jones is overcome.") (emphasis in original). The Examiner asserts, however, that the claim language can be interpreted to encompass an allocation that occurs at the receiver and is directed to the transmitter. Appellants respectfully disagree.

Appellants maintain that the limitation of "allocating at the link transmitter the plurality of data credits to a plurality of logical channels" means that the link transmitter is performing the allocation. This is specifically discussed at page 6, line 28 to page 7, line 6 of the Application, where the advantages of the claimed system and method over the prior art, such as Jones, is discussed. Furthermore, the Examiner fails to discuss independent claim 9 in which it is clear that the link transmitter performs the allocation ("the link transmitter allocates a plurality of data credits to a plurality of logical channels").

The Examiner has rejected claims 1-5, 7-12, 14-20 and 22-23 under 35 U.S.C. 103(a) as being unpatentable over Bloch in view of Jones and in further view of Takase. The Examiner's rejection of claims 2-5, 7-8, 10-12, 14-15, 17-20 and 22-23 relies upon the rejections of claims 1, 9 and 16. Appellants respectfully submit that claims 1, 9 and 16 distinguish over the Bloch/Jones/Takase combination, as discussed above, and also submit that claims 2-5, 7-8, 10-12, 14-15, 17-20 and 22-23, which depend from claims 1, 9 and 16, distinguish over the Bloch/Jones/Takase combination for the same reasons.

B. Conclusion

For the foregoing reasons, Appellants respectfully request that the Board direct the Examiner in charge of this examination to withdraw the rejections.

Please charge any fees required in the filing of this appeal to Deposit Account 08-0750.

VIII. Claims Appendix

A copy of the claims involved in this appeal, namely claims 1-5, 7-12, 14-20 and 22-23, is attached as a Claims Appendix.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.

Respectfully submitted,

Dated: November 6, 2008

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VIII. Claims Appendix

1. A method, comprising:

providing from a link a receiver a plurality of data credits to a link transmitter;

allocating at the link transmitter the plurality of data credits to a plurality of logical channels;

transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link, wherein the ingress link has a forward link and a reverse link, and wherein the plurality of packets are transmitted on the forward link;

storing the plurality of packets in a plurality of receiver buffers at the link receiver;

updating a free buffer pool at the link receiver; and

transmitting a flow control packet from a link receiver to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.

2. The method of claim 1, wherein the link receiver updating the free buffer pool at the link receiver comprises the link receiver updating the free buffer pool as one of the plurality of packets is transmitted out of the plurality of receiver buffers.

3. The method of claim 1, wherein the flow control packet notifies the link transmitter of an empty portion of the plurality of receiver buffers.

4. The method of claim 1, wherein one of the plurality of data credits corresponds to one of the plurality of receiver buffers being empty.

5. The method of claim 1, further comprising selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter.

6. (Cancelled)

7. The method of claim 1, wherein the link transmitter and the link receiver operate in a switch fabric network.

8. The method of claim 7, wherein the switch fabric network is one of an Infiniband network and a Serial RapidIO network.

9. A switch, comprising:

a plurality of receiver buffers coupled to receive a packet from a link transmitter on an ingress link having a forward link and a reverse link after the link transmitter allocates a plurality of data credits to a plurality of logical channels, wherein the packet is stored in the plurality of receiver buffers;

a free buffer pool; and

a link receiver flow control algorithm, wherein the link receiver flow control algorithm transmits a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.

10. The switch of claim 9, wherein the flow control packet notifies the link transmitter of an empty portion of the plurality of receiver buffers.

11. The switch of claim 9, wherein one of the plurality of data credits corresponds to one of the plurality of receiver buffers being empty.

12. The switch of claim 9, wherein the link transmitter selects to which of the plurality of logical channels to allocate the additional data credits.

13. (Cancelled)

14. The switch of claim 9, further comprising a link receiver, wherein the link transmitter and the link receiver operate in a switch fabric network.

15. The switch of claim 14, wherein the switch fabric network is one of an Infiniband network and a Serial RapidIO network.

16. A computer-readable medium encoded with_computer executable instructions for instructing a processor to perform a method of updating a link transmitter, the instructions comprising:

providing from a link a receiver a plurality of data credits to a link transmitter;

allocating at the link transmitter the plurality of data credits to a plurality of logical channels;

transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link, wherein the ingress link has a forward link and a reverse link, and wherein the plurality of packets are transmitted on the forward link;

storing the plurality of packets in a plurality of receiver buffers at the link receiver;

updating a free buffer pool at the link receiver; and

transmitting a flow control packet from a link receiver to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.

17. The computer-readable medium of claim 16, wherein the link receiver updating the free buffer pool comprises the link receiver updating the free buffer pool as one of the plurality of packets is transmitted out of the plurality of receiver buffers.

18. The computer-readable medium of claim 16, wherein the flow control packet notifies the link transmitter of an empty portion of the plurality of receiver buffers.

19. The computer-readable medium of claim 16, wherein one of the plurality of data credits corresponds to one of the plurality of receiver buffers being empty.

20. The computer-readable medium of claim 16, further comprising selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter.

21. (Cancelled)

22. The computer-readable medium of claim 16, wherein the link transmitter and the link receiver operate in a switch fabric network.

23. The computer-readable medium of claim 20, wherein the switch fabric network is one of an Infiniband network and a Serial RapidIO network.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.